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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,772	09/12/2003	Makoto Shizukuishi	107317-00061	5771

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EXAMINER

LIVEDALEN, BRIAN J

ART UNIT PAPER NUMBER

2878

DATE MAILED: 05/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/660,772

Applicant(s)

SHIZUKUISHI, MAKOTO

Examiner

Brian J. Livedalen

Art Unit

2878

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 April 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 7-20 and 23-26 is/are allowed.
- 6) ☒ Claim(s) 1, 5 and 6 is/are rejected.
- 7) ☒ Claim(s) 2-4, 21 and 22 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 4/24/2006.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

This action is in response to amendment filed 4/24/2006. Claims 1-26 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hagiwara (JP 08340100) in view of Abe (2001/0054726).

In regard to claim 1, Hagiwara discloses (fig. 2) a solid state image pickup device having a semiconductor substrate having a first layer of a first conductivity type (21); a second layer of a second conductivity type opposite to the first conductivity type (22), the second layer being formed on the first layer in the semiconductor substrate; a first region (23) of the first conductivity type formed in the second layer and constituting a photodiode with the second layer, the first region being electrically floating and capable of storing charges (page 3, paragraphs 0014, 0015); a first gate structure including a charge storage region (13) and a control gate (14), the first gate structure being formed on a surface of the semiconductor substrate adjacent to a portion of the first region, and the charge storage region being electrically isolated (28) from the first region; a second region of the first conductivity type (25) formed in the second layer adjacent to the first gate structure on a side opposite to the first region, and constituting a non-volatile

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memory element with the first region and the first gate structure, and a first wiring connected to the second region for applying a voltage (V_{ro}) to the second region (page 3, paragraphs 0016- 0018); and a control circuit for applying a first write voltage to the control gate of the first gate structure, the first write voltage being a write voltage for tunneling and injecting charges accumulated in the first region into the charge storage region (page 3, paragraph 0018). Hagiwara fails to disclose a light shielding film above the first gate structure and an aperture above the first region. However, Abe discloses (fig. 1) a solid-state image pickup device with a light shielding film above a gate structure and an aperture above the image pickup region (page 3, paragraph 0056). It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a light shielding film and aperture in order to eliminate noise due to light impinging on the gate structure.

In regard to claim 5, Hagiwara discloses that the charge storage region of the non-volatile memory element has a floating gate (page 3, paragraph 0018).

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hagiwara (JP 08340100) in view of Abe (2001/0054726) as applied to claim 1, and in further view of Nakai (6784933).

In regard to claim 6, Hagiwara discloses the charge storage region has an interface with an insulating layer. Hagiwara fails to disclose the interface being between a silicon nitride film and a silicon oxide film. However, Nakai discloses a solid-state image pickup device with non-volatile memory using a control gate with a charge

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storage region having an interface between a silicon nitride film and a silicon oxide film (column 12, lines 21-31). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use silicon nitride and silicon oxide films as the insulating layer in order to more effectively trap the charge in the charge storage layer.

Allowable Subject Matter

Claims 2-4, 21, and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Claims 2-4, 21, and 22 are neither anticipated nor made obvious by the prior art of record.

In regard to claim 2, the prior art of record fails to disclose the device set forth in combination with a control circuit that applies a second write voltage, the second write voltage being a write voltage for injecting charges as hot carrier injection.

In regard to claim 3, the prior art of record fails to disclose the device set forth in combination with a second gate structure of an insulated type formed adjacent to the first region; and a third region of the first conductivity type adjacent to the gate structure opposite the first region, and the third region, second gate structure, and first region constitute an insulated gate type transistor.

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In regard to claim 4, the prior art of record fails to disclose the device set forth in combination with a fourth region of the first conductivity type projecting from an upper surface of the first layer into the second layer.

In regard to claim 21, the prior art of record fails to disclose the device set forth in combination with a second wiring connected to the first layer for applying a reset voltage from a voltage source to extinguish a potential barrier in the second layer and clear charges accumulated in the first region.

In regard to claim 22, the prior art of record fails to disclose the device set forth in combination with a fifth region of the second conductivity type, formed in a surface portion of the first region.

Claims 7-20 and 23-26 are allowed.

The following is an examiner's statement of reasons for allowance: Claims 7-20 and 23-26 are neither anticipated nor made obvious by the prior art of record.

In regard to claims 7-10, 23, and 24, the prior art of record fails to disclose a solid state image pickup device having a semiconductor substrate having a first layer of a first conductivity type; a second layer of a second conductivity type opposite to the first conductivity type, the second layer being formed on the first layer in the semiconductor substrate; a first region of the first conductivity type formed in the second layer and constituting a photodiode with the second layer, the first region being electrically floating and capable of storing charges; a first gate structure including a charge storage region and a control gate, the first gate structure being formed on a surface of the

semiconductor substrate adjacent to a portion of the first region, and the charge storage region being electrically isolated from the first region; a second region of the first conductivity type formed in the second layer adjacent to the first gate structure on a side opposite to the first region, and constituting a non-volatile memory element with the first region and the first gate structure, and a first wiring connected to the second region for applying a voltage to the second region; and a control circuit for applying a first write voltage to the control gate of the first gate structure, the first write voltage being a write voltage for tunneling and injecting charges accumulated in the first region into the charge storage region, a light shielding film above the first gate structure and an aperture above the first region, and a second gate structure of an insulated type formed adjacent to the first region; and a third region of the first conductivity type adjacent to the gate structure opposite the first region, and the third region, second gate structure, and first region constitute an insulated gate type transistor.

In regard to claims 11-20, 25, and 26, the prior art of record fails to disclose a solid state image pickup device having a semiconductor substrate having a first layer of a first conductivity type; a second layer of a second conductivity type opposite to the first conductivity type, the second layer being formed on the first layer in the semiconductor substrate; a first region of the first conductivity type formed in the second layer and constituting a photodiode with the second layer, the first region being electrically floating and capable of storing charges; a first gate structure including a charge storage region and a control gate, the first gate structure being formed on a surface of the semiconductor substrate adjacent to a portion of the first region, and the

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charge storage region being electrically isolated from the first region; a second region of the first conductivity type formed in the second layer adjacent to the first gate structure on a side opposite to the first region, and constituting a non-volatile memory element with the first region and the first gate structure, and a first wiring connected to the second region for applying a voltage to the second region; and a control circuit for applying a first write voltage to the control gate of the first gate structure, the first write voltage being a write voltage for tunneling and injecting charges accumulated in the first region into the charge storage region, a light shielding film above the first gate structure and an aperture above the first region, and a control circuit for supplying a forward bias voltage to the first layer of the semiconductor substrate to supply current to the nonvolatile memory element.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

Applicant's arguments with respect to claims 1, 5, and 6 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments, see pages 13-17, filed 4/24/2006, with respect to claims 2-4 and 7-26 have been fully considered and are persuasive.

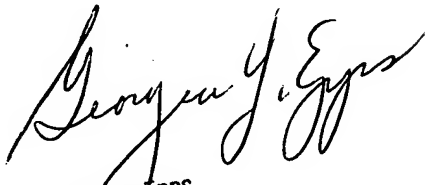
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian J. Livedalen whose telephone number is (571) 272-2715. The examiner can normally be reached on 8:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps can be reached on (571) 272-2328. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

bjl


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